REMARKS

Attached hereto is a marked up version of the changes made in the specification and claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**"

Claims 1-5, and 14 are all of the claims pending in the present Application. Claims 6-13 are canceled above in response to the Election/Restriction requirement of the first Office Action dated July 11, 2001. New claim 14 is added to reflect the embodiment taught in Figure 7 and described in the specification beginning at line 7 of page 15. The advantage of this second embodiment is that the PAE layer reduces capacitance between copper wires and the HSQ layers provide containment.

Claims 1-5 stand rejected under 35 USC §112, second paragraph, as being indefinite. Claims 1 and 2 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,096,648 to Lopatin et al. Claims 3-5 stand rejected under 35 USC §103(a) as unpatentable over Lopatin, further in view of US Patent 6,037,664 to Zhao et al.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, the present invention is directed to a semiconductor device having an HSQ layer formed on a copper wiring line and having properties that copper is unlikely to enter the HSQ layer. A plug is formed in the HSQ layer and connected to the copper wiring line and a copper wiring line is inserted into the HSQ layer and connected to the plug. A W layer which allows the plug and HSQ layer to adhere to each other is formed

between the plug and HSQ layer.

II. THE 35 USC §112, Second Paragraph, Rejection

Claims 1-5 stand rejected under 35 U.S.C. §112, second paragraph. The claims have been amended, above, to overcome this rejection. Specifically, claim 3 has been reworded to eliminate one of the phrases "between one of said plurality" and claims 3-5 have been revised to refer to "at least one layer" rather than "layer".

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTION

The Lopatin et al. Reference (US Patent 6,096,648)

Lopatin et al. discloses a method of metallizing a semiconductor chip with copper, in which a low dielectric constant layer is deposited on the semiconductor chip to fill the gaps between the newly created copper conductive lines.

The Examiner asserts that, relative to claims 1 and 2, Lopatin et al.:

> *... teach copper 24 and low dielectric constant layer, e.g., layer 30 including HSQ material thus possessing the property that Cu is unlikely to enter it since the same material is employed. ...Although Lopatin et al. do not explicitly recite the Cu concentration to be equal or higher than 10 ^{19} atoms/cm^3, such would have been encompassed in Lopatin et al. since the concentration therein is not required or limited to be below the said value, and since the optimization of such concentration to obtain a desired conductivity would have been obvious to one skilled in the art....*

Although Lopatin teaches HSQ in lines 27-28 of column 6, it fails to teach the concentration of Cu as being equal to or higher than 10^{19} atoms/cm^3. Additionally, Lopatin teaches a barrier layer 54 (Figure 8, column 7 at lines 5-9), and Zhao demonstrates such

barrier is even considered in the art as being absolutely necessary (column 4 at lines 47-52, 63). Therefore, neither Lopatin nor Zhao seems to take the view that Cu is unlikely to enter the HSQ layer. In contrast, by adopting such view, the narrow pitches of 0.2 to 0.3 μm obtainable by the present invention (see specification page 9 at lines 7-8) are realizable.

The specification of the present invention on page 8 at lines 12-14 explicitly shows that the HSQ layer possesses the property that Cu is unlikely to enter the insulating layer. Further, on page 11 at lines 17-20, it is explained "if the Cu concentration in the insulating film reaches some point on the order of 10^{19} atoms/cm^3, the leakage current has some influence on the operations of the semiconductor device". Additionally, on page 12 at lines 8-12, it is explained that if the interlayer insulating film is formed of HSQ, the Cu concentration of the Cu wiring line can be set at or higher than 10^{19} atoms/cm^3.

In contrast, Lopatin makes no disclosure concerning the relationship between concentration of Cu entering the interlayer insulating film and the operation of the semiconductor device, especially at closer separation distance between the Cu lines.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... a plurality of wiring lines which are formed of Cu whose concentration is equal to or higher than 10^{19} atoms/cm^3; and an insulating layer which has a property that Cu is unlikely to enter said insulating layer", as required by claim 1.

Relative to claim 4, the Examiner admits that Lopatin fails to teach or suggest the same etching rate but asserts that

... Zhao et al. teach various the conventional use of liner in conjunction with copper wherein the barrier also provides adhesion, including the use of tungsten for such material.... The selection of the same etching rate would have been obvious and would have been within the purview of one skilled in the art to facilitate the removal of the wiring line and the adhesion/barrier layer.

The Examiner's motivation to incorporate an adhesion layer having the same etch rate as the copper line is a conclusory statement that merely states the result of using similar etch rates. There is no suggestion in either reference that etch rates are even a manufacturing concern, let alone a concern to match rates for various components on the device, especially the specific components identified in the present invention. The conclusory statement fails even to provide an indication that the problem was recognized in the art at the time of the invention. For this reason, Applicant respectfully asserts that the rejection for claim 4 fails as a prima facie rejection.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... wherein each of said at least one adhesion layer has an etching rate which is essentially equivalent to an etching rate of said plurality of wiring lines", as required by claim 4.

Relative to claim 5, in spite of the Examiner's characterization, the prior art on the record relied upon by the Examiner actually teaches against use of tungsten (W) as the adhesion layer for copper, as clearly indicated at lines 26-27 of column 5 of Zhao et al.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Lopatin et al. and/or Zhao et al. fails to teach or suggest the claimed invention.

IV. Formal matters and Conclusion

The Examiner requested that Applicant re-file the IDS filed on July 27, 2000. In response, Applicant is unable to find a record that any IDS has been filed in this Application as of this date and would suggest that the indication in the USPTO file is an error.

In view of the foregoing, Applicant submits that claims 1, 2, 5, and 14-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/14/01

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 2 - 5 have been amended, as follows:

2. (Amended) The semiconductor device according to claim 1, wherein said insulating layer [includes an] comprises HSQ [layer which is formed of HSQ] (Hydrogen Silsesquioxane).

3. (Amended) The semiconductor device according to claim 2, further comprising at least one adhesion layer[s, which are] formed [respectively] in an interface between [one of] said plurality of wiring lines and said insulating layer [and between one of said plurality of wiring lines and said insulating layer,] and [which allow] allowing said plurality of wiring lines and said insulating layer to adhere to one another [through said adhesion layers].

4. (Amended) The semiconductor device according to claim 3, wherein each of said at least one adhesion layer has an etching rate which is essentially equivalent to an etching rate of said plurality of wiring lines.

5. (Amended) The semiconductor device according to claim 4, wherein at least one of said at least one adhesion layer [is formed of] comprises tungsten.